PVP 20

Code: 20EC3302

II B.Tech - I Semester – Regular / Supplementary Examinations
DECEMBER 2023

DIGITAL LOGIC DESIGN
(ELECTRONICS & COMMUNICATION ENGINEERING)

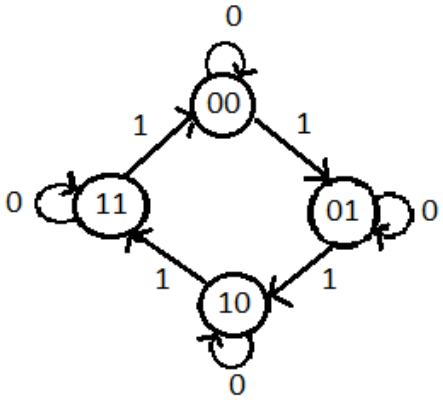
Duration: 3 hours Max. Marks: 70

Note: 1. This paper contains questions from 5 units of Syllabus. Each unit carries 14 marks and have an internal choice of Questions.
2. All parts of Question must be answered in one place.

BL – Blooms Level CO – Course Outcome

			BL	CO	Max. Marks
UNIT-I					
1	a)	Convert the $(101101.1101)_2$ number into Decimal, Hexadecimal and octal form.	L2	CO1	7 M
	b)	State and Prove De Morgan's Theorems using truth table.	L2	CO1	7 M
OR					
2	a)	Explain about any four binary codes.	L2	CO1	7 M
	b)	The Hamming code 101101101 is received. Correct it if any errors are available. Where 4 parity bits are used.	L2	CO1	7 M
UNIT-II					
3	a)	Simplify the following Boolean function for minimal SOP form using K–Map method. F (A, B, C, D) =∑m (0,1,2,3,5,7,8,9,11,14)	L3	CO2	7 M

	b)	Find the dual and complement for the following function F=ABC+A'B'C'+AB'C'+A'BC+AB'C	L3	CO2	7 M
OR					
4	a)	Convert F (X, Y, Z) = X'Y + X'Z + YZ into canonical SOP form.	L2	CO2	6 M
	b)	Simplify the following Boolean equation using K-map. F(W,X,Y,Z)=∑m(0,7,8,9,10,12) + ∑d (2,5,13). Implement the simplified expression using NAND Gates.	L3	CO2	8 M
UNIT-III					
5	a)	Design 3 to 8 decoder using 2 to 4 decoders and OR gate.	L4	CO3	7 M
	b)	Design 16x1 Mux using 4x1 Multiplexers.	L4	CO3	7 M
OR					
6	a)	Design 4-bit Binary Adder/Subtractor circuit with neat sketches.	L4	CO3	8 M
	b)	Implement the function F (A, B, C) =∑m (1, 3, 5, 6) using 2x1 Mux.	L3	CO3	6 M
UNIT-IV					
7	Summarize the SR, JK, D & T flip-flops with its characteristic and Excitation tables.		L2	CO4	14 M
OR					
8	a)	Explain about SIPO shift Register with neat sketches.	L2	CO4	7 M
	b)	Outline about the steps in synchronous counters design.	L2	CO4	7 M

<table>
<tr><td colspan="6">UNIT-V</td></tr>
<tr><td rowspan="2">9</td><td>a)</td><td>Explain about the Analysis of clocked sequential circuits with an Example.</td><td>L4</td><td>CO5</td><td>7 M</td></tr>
<tr><td>b)</td><td>Design the following synchronous sequential circuit using T Flip-Flops.
 
</td><td>L2</td><td>CO5</td><td>7 M</td></tr>
<tr><td colspan="6">OR</td></tr>
<tr><td>10</td><td colspan="2">
<table>
<tr><td rowspan="2">PS</td><td colspan="2">NS, Z</td></tr>
<tr><td>X=0</td><td>X=1</td></tr>
<tr><td>A</td><td>B,1</td><td>H,1</td></tr>
<tr><td>B</td><td>F,1</td><td>D,1</td></tr>
<tr><td>C</td><td>D,0</td><td>E,1</td></tr>
<tr><td>D</td><td>C,0</td><td>F,1</td></tr>
<tr><td>E</td><td>D,1</td><td>E,1</td></tr>
<tr><td>F</td><td>C,1</td><td>E,1</td></tr>
<tr><td>G</td><td>C,1</td><td>D,1</td></tr>
<tr><td>H</td><td>C,0</td><td>A,1</td></tr>
</table>
For the above state table obtain the following
i. Draw the corresponding state diagram
ii. Tabulate the reduced state table
iii. Draw the state diagram corresponding to the reduced state table.</td><td>L4</td><td>CO5</td><td>14 M</td></tr>
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